IN THE CLAIMS:

1. (Original). An ink jet printer comprising a printer cartridge containing a printhead attached to a cartridge carriage for translation of the cartridge across a print media, an off carriage ink supply, a printer microprocessor, and a combined ink fill tube and electrical connection cable connected between the cartridge and the off carriage ink supply for providing refill ink to the ink cartridge and control of the carriage and printhead.

2. (Original) The ink jet printer of claim 1 wherein the combined ink fill tube and electrical connection cable is attached to the carriage and a refill tube is connected between the cartridge and carriage for providing ink to the cartridge.

3. (Original) The ink jet printer of claim 1 wherein the ink cartridge further comprises a cartridge body containing an ink reservoir and a pressure regulator for controlling refill of the ink reservoir within the cartridge body.

4. (Original) The ink jet printer of claim 3 wherein the pressure regulator comprises gas filled microcapsules.

5. (Original) The ink jet printer of claim 1 wherein the printhead contains ink ejectors for ejecting a mass of ink ranging from about 0.2 to about 1 nanogram.

6. (Original) The ink jet printer of claim 1 wherein the printhead comprises an ultra-thin semiconductor material having a thickness ranging from about 10 microns to less than about 500 microns.

7. (Original) The ink jet printer of claim 1 wherein the printhead comprises a shelf-less heater chip having ink channels etched into a surface of the chip.

8. (Currently Amended) A printhead for an ink jet printer comprising a semiconductor substrate, a first insulating layer deposited on the substrate, a first conductive layer deposited

on the insulating layer, wherein the first conductive layer is etched to define an ink ejector location between opposed portions of the first conductive layer, a diamond-like-carbon (DLC) layer deposited in the ink ejector location and on at least a portion of the first conductive layer, a second insulating layer deposited on the opposed portions of the first conductive layer, and a second conductive layer deposited on at least a portion of the second insulating layer, wherein the DLC layer contains an upper doped ~~or undoped~~ layer and a lower layer doped with a material different than the doping material of the upper layer which is sufficient to provide increasing conductivity thereto thereby defining ink ejection devices.

9. (Original) The printhead of claim 8 wherein the DLC layer comprises a boron-doped DLC layer portion deposited in the ink ejector location and a silicon-doped DLC layer portion provided as an island substantially between the opposed portions of the first conductive layer.

10. (Canceled)

11. (Original) The printhead of claim 8 further comprising a smoothing layer deposited on the upper DLC layer.

12. (Original) The printhead of claim 8 wherein the ink ejector is configured for ejecting a mass of ink ranging from about 0.2 to about 1 nanogram.

13. (Original) The printhead of claim 8 wherein the second insulating layer comprises an intermetal dielectric layer made of DLC having a thickness ranging from about 1000 to about 3000 angstroms.

14. (Original) A printhead for an ink jet printer comprising a semiconductor substrate having a device surface including a first insulating layer deposited on the substrate, a resistive layer deposited on the first insulating layer, a first conductive layer deposited on the resistive layer, wherein the first conductive layer is etched to define an ink ejector location between opposed portions of the first conductive layer, a diamond-like-carbon (DLC) protective layer

deposited on the device surface over the first insulating, resistive and first conductive layers, a second insulating layer deposited on the opposed portions of the first conductive layer, and a second conductive layer deposited on at least a portion of the second insulating layer, wherein a portion of the DLC protective layer is doped to improve adhesion between the first conductive layer and the second insulating layer.

15. (Original) The printhead of claim 14 wherein the DLC protective layer is doped with titanium in the ink ejector location to provide enhanced corrosion resistance.

16. (Original) The printhead of claim 14 wherein the DLC protective layer comprises a lower silicon doped (DLC) layer and an upper undoped DLC layer.

17. (Original) The printhead of claim 14 wherein ink ejectors in each ink ejector location are configured for ejecting a mass of ink ranging from about 0.2 to about 1 nanogram.

18. (Original) The printhead of claim 14 wherein the second insulating layer comprises an intermetal dielectric layer made of DLC having a thickness ranging from about 1000 to about 3000 angstroms.

19. (Original) The printhead of claim 14 wherein the semiconductor substrate has a thickness ranging from about 600 to about 650 microns.

20. (Original) The printhead of claim 14 wherein the semiconductor substrate has a thickness ranging from about 10 to less than about 500 microns.

21. (Original) The printhead of claim 14 wherein the semiconductor substrate comprises a non-epitaxial silicon substrate.

22. (Original) An ink jet printhead having low flow resistance features comprising, a flow feature portion of a printhead attached to a semiconductor substrate containing ink

ejectors, the flow feature portion containing ink channels and ink chambers, wherein the ink channels contain a tapered area adjacent an ink feed edge of the chip and a feed channel between the tapered area and the ink chambers, the tapered area having a first entrance width adjacent the ink feed edge of the chip and the feed channel having a second entrance width, wherein a ratio of the first entrance width to second entrance width ranges from about 2:1 to about 8:1.

23. (Original) The ink jet printhead of claim 22 wherein the tapered area has a first length and the feed channel has a second length, and wherein a ratio of the first length to the second length ranges from about 1:1 to about 7:1.

24. (Original) The ink jet printhead of claim 23 further comprising a shelf length, the shelf length including an area between the ink feed edge of the chip and the tapered area, wherein the shelf length is less than about 29 microns in length.

25. (Original) The ink jet printhead of claim 22 further comprising a shelf length, the shelf length including an area between the ink feed edge of the chip and the tapered area, wherein the shelf length is less than about 29 microns in length.

26. (Original) The ink jet printhead of claim 22 wherein the ink chambers comprise chamber walls and the ink ejector is a heater resistor having a heater edge, and wherein a distance from the heater edge to the chamber wall around a periphery of the heater resistor is about 2 microns or less.

27. (Original) The ink jet printhead of claim 22 wherein the semiconductor substrate comprises a silicon chip made from a single crystal silicon wafer having a thickness ranging from about 500 to about 1000 microns.

28. (Original) The ink jet printhead of claim 27 wherein the silicon wafer has a thickness ranging from about 680 to about 900 microns.

29. (Original) A printhead for an ink jet printer comprising a semiconductor chip containing a plurality of heater resistors for ink ejection, a power field effect transistors (FET's) for driving each heater resistor, and CMOS logic devices coupled to the FET's and heater resistors, wherein a gate oxide layer for gates of the FET's has a thickness greater than a gate oxide layer for gates of the CMOS logic devices.

30. (Original) The printhead of claim 29 wherein the chip further comprises a plurality of fuses as memory elements, the fuses being formed from a tantalum tantalum/aluminum composite material.

31. (Original) The printhead of claim 30 further comprising a passivation material deposited on the fuses, wherein the passivation material comprises a spun-on-glass material.

32. (Original) The printhead of claim 30 further comprising passivation layers deposited on the fuses, wherein the passivation layers comprise at least one silicon dioxide layer and at least one spun-on-glass layer.

33. (Original) The printhead of claim 29 wherein the FET's gate oxide thickness ranges from about 200 to about 400 Angstroms.

34. (Original) The printhead of claim 33 wherein the CMOS logic devices' gate oxide thickness ranges from about 100 to about 200 Angstroms.

35. (Original) The printhead of claim 29 wherein the FET's have an on resistance of less than about 100,000 ohm-μm2/A, where A is a surface area of each of the FET's.

36. (Original) An ink jet printhead comprising a semiconductor substrate containing an ink ejector thereon, the ink ejector having an ink contact surface, and a nozzle plate attached to the semiconductor substrate, wherein the nozzle plate contains ink ejection nozzles have a

truncated substantially conical shape, a cone angle, an entrance, an exit, a length between the entrance and exit, and a nozzle volume per unit length of greater than one defined by the length, cone angle, and cross-sectional area of the nozzle, and wherein a distance from the ink contact surface of the ink ejector to the exit of the nozzle is less than about 37 microns.

37. (Original) A semiconductor substrate for a micro-fluid ejection device comprising a silicon chip made from a single crystal silicon wafer wherein the wafer has a thickness ranging from about 500 to about 1000 microns and containing a plurality of ink ejection devices defined on a surface of the chip.

38. (Currently Amended) A semiconductor substrate for a micro-fluid ejection device comprising a ~~silicion~~ silicon chip made from a flexible single crystal silicon wafer wherein the wafer has a thickness ranging from about 50 to about 400 microns and containing a ~~pluarlity~~ plurality of ink ejection devices defined on a surface of the chip.